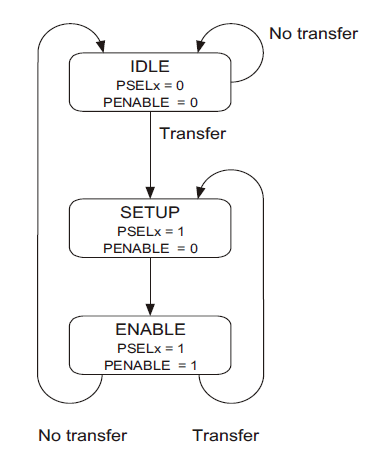
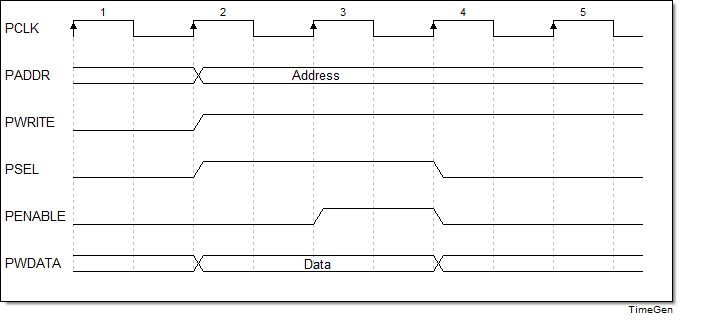
# State diagram



# Write transfer



Clock cycle 2: (SETUP)

Address, write signal, select signal and data on bus.

Clock cycle 3: (ENABLE)

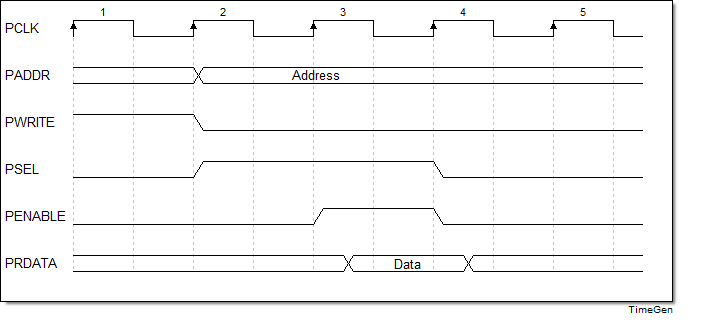
Enable signal on bus.

APB slave:

For a write transfer the data can be latched at the following points:

* on either rising edge of PCLK, when PSEL is HIGH.
* on the rising edge of PENABLE, when PSEL is HIGH.

# Read transfer



Clock cycle 2: (SETUP)

Address, write signal, select signal on bus.

Clock cycle 3: (ENABLE)

Enable signal, data on bus.

APB slave:

For read transfers the data can be driven on to the data bus when PWRITE is LOW and

both PSELx and PENABLE are HIGH. While PADDR is used to determine which

register should be read.

APB bridge:

The data is sampled on the rising edge of clock at the end of the ENABLE cycle.